

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application.

**Listing of Claims:**

Please amend the claims as follows:

Claims 1-35 (Canceled)

36. (Currently Amended) An apparatus for delaying an audio signal comprising:
- a first FIFO register receptive to a digital audio signal, the digital audio signal having an associated clock signal;
  - an audio format detection circuit coupled to the first FIFO register and operative to detect a format of the digital audio signal by analyzing the associated clock signal;
  - a memory controller coupled to the FIFO register;
  - a memory chip coupled to the memory controller;
  - a write address generator coupled to the audio format detection circuit and memory controller;
  - a read address generator coupled to the memory controller; and
  - a second FIFO register coupled to the memory controller and operative to provide a time delay in the digital audio signal the duration of which is related to the detected format of the digital audio signal.
37. (Previously Presented) The apparatus as claimed in claim 36, wherein the digital audio signal further comprises a serial audio clock signal and a plurality of accompanying signals.
38. (Previously Presented) The apparatus as claimed in claim 37, wherein the accompanying signals further comprises a data signal and a frame synchronization signal.

39. (Currently Amended) The apparatus as claimed in claim 37, wherein the audio format detection circuit is operable to detect a number of edge transitions in the serial audio clock signal and provide a corresponding detected count.
40. (Currently Amended) The apparatus claimed in claim 37, wherein the audio format detection circuit further comprises a plurality of model data, wherein each model data represents one of a plurality of audio signal formats and a corresponding one of a plurality of time delay data, wherein the detected count is compared to the model data, the audio format detection circuit operable to provide the delay data representing the model data that is equal to the detected count.
41. (Previously Presented) The apparatus as claimed in claim 40, wherein the processed clock signal is synchronized to a reference clock.
42. (Currently Amended) The apparatus as claimed in claim 37, wherein the audio format detection circuit is operable to provide a processed clock signal by dividing the serial clock signal by a constant.
43. (Previously Presented) The apparatus according to claim 42, wherein the processing is operable to compare a new time delay data to an old time delay data, the processing device operable to reconfigure a buffer if the new time delay data is not equal to the old time delay data.
44. (Previously Presented) The apparatus as claimed in claim 40, wherein the detected count is compared to the model data by a plurality of comparators.
45. (Previously Presented) The apparatus as claimed in claim 40, wherein the provided time delay data is a first offset value, the processing device operable to resize a write address pointer with the offset value.
46. (Previously Presented) The apparatus as claimed in claim 40, wherein the provided time delay data is a second offset value, the processing device operable to resize a read address pointer with the offset value.

47. (Previously Presented) The apparatus as claimed in claim 40, wherein the processing device further comprises a memory unit to provide the time delay corresponding to the time delay data.

48. (Previously Presented) The apparatus as claimed in claim 45, wherein the processing device further comprises a first parameter and a second parameter, the first parameter configured accordingly to the provided time delay data.

49. (Previously Presented) The apparatus as claimed in claim 48, wherein the first parameter is a write address parameter, the second parameter is a read address parameter, and the memory unit is a buffer.

50. (New) The apparatus as claimed in claim 37, wherein the audio format detection circuit comprises a synchronization circuit operative to synchronize the serial audio clock and a reference clock and, an edge detection circuit operative to detect edge transitions in the synchronized serial and reference clock.

51. (New) The apparatus as claimed in claim 50, wherein the audio format detection circuit comprises a memory lookup operative to obtain a memory address according to the detected edge transitions and correlating to the audio format of the digital audio signal, the memory address used to configure the write address generator.

52. (New) The apparatus as claimed in claim 37, wherein the format of the digital audio signal is one of eight possible formats.

53. (New) A method comprising:

receiving a digital audio signal;

analyzing a clock signal associated with the digital audio signal to determine a audio format of the digital audio signal;

providing an audio signal delay according to the audio format of the digital audio signal; and

outputting the digital audio signal.

54. (New) A method as recited in claim 53, further comprising:

detecting a resulting value from a clock signal synchronized with the digital audio signal and a reference clock;

latching the resulting value;

looking up a memory write address using the resulting value;

comparing the memory write address to a previous memory write address; and

if the memory write address is unequal to the previous memory write address, then retrieving a new audio signal delay.

55. (New) A method as recited in claim 53, further comprising counting transitions of a reference clock to create the resulting value.

56. (New) A method as recited in claim 53, further comprising counting transitions of a reference clock during a period of a modified clock signal derived from the clock signal.

57. (New) An apparatus comprising:

means for receiving a digital audio signal;

means for analyzing a clock signal associated with the digital audio signal to determine a audio format of the digital audio signal;

means for implementing audio signal delay by the audio format of the digital audio signal; and

means for outputting the digital audio signal.